

III-V COMPOUND SEMICONDUCTOR SELECTIVE AREA EPITAXY ON SILICON  
SUBSTRATES

BY

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THESIS

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## ABSTRACT

In electronics, the integration of III-V compound semiconductor materials and silicon is a way to solve the silicon feature size limit and power consumption problems given the high electron mobility that the III-V semiconductors have. Higher electron transport properties than silicon enable the electronic devices made of III-V materials to perform at higher switching speed. The integration of III-V semiconductor devices on silicon is the most approachable way that utilizes both the mature manufacturing technology of silicon CMOS circuits and the good electronic properties of III-V material. In optoelectronics, silicon is not a good material to make light sources because of its indirect bandgap. The potential high bandwidth and high speed data transmission in VLSI optical interconnects drive the need for optical device integration in silicon circuits. Monolithic III-V on silicon substrate optoelectronic devices are a promising direction to achieve optical data transmission on chip.

Selective area epitaxy is an MOCVD/MBE growth method that deposits high quality epitaxial materials on selected substrate surface areas. The selectivity is achieved by using  $\text{SiO}_2$  or  $\text{Si}_3\text{N}_4$  as a growth mask, so that epitaxial growth only happens on exposed substrate surface. The dislocation density reduction and bottom-up fabrication advantages of selective area epitaxy make it a widely used approach in III-V on silicon integration. This thesis introduces the motivation, growth methods, issues, and applications of III-V semiconductor selective area epitaxy on silicon substrate.

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# 1. INTRODUCTION

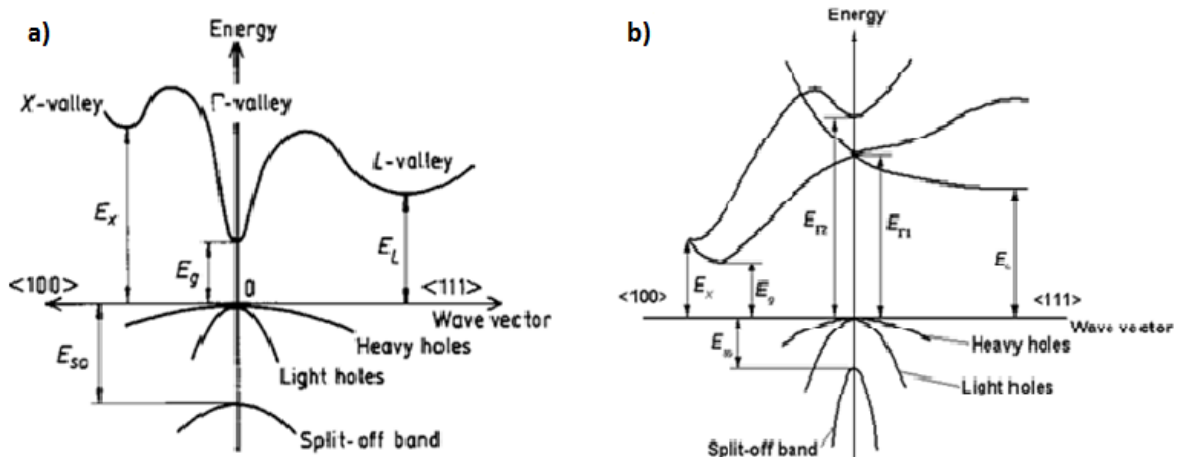
## 1.1 Motivation for III-V Compound Semiconductor Growth on Si Substrates

Monolithic integration of compound semiconductor devices and silicon devices on a single substrate is a possible way to achieve significant improvement in the performance of very large scale integrated (VLSI) circuits and optoelectronic devices.

Silicon is the predominant material in the semiconductor industry. It is abundant, cheap and robust. After more than a half century of development, the silicon fabrication process has been perfected and is mature. However, recently, with continuous decrease of feature size in VLSI circuits and the rapid development of optoelectronics, two issues arise and cast doubt on the future of the silicon industry. One is the feature size limitation, and the other is the indirect bandgap of silicon.

In the past 20 years, the feature size on Si substrates has already decreased more than 40 times. The reduction of individual feature size enables denser integration of electronic elements on the same area of silicon wafer. According to recent research, the feature size on Si substrates is decreasing towards sub-10 nm [1]. It is a challenging task to continue this trend, which requires a breakthrough in the current state-of-the-art semiconductor fabrication technology. The suggested routes to solve this feature size limitation problem are either finding a revolutionary fabrication method to further decrease the size of patterns on Si integrated circuits or switching to a new material platform that has better electronic and (or) optoelectronic properties than Si. Both of these routes have shortcomings and obstacles to overcome. For the first route, extreme ultraviolet lithography (EUVL) has the potential to

further decrease the feature size on Si integrated circuits below 10 nm [2]. However, challenges exist in many aspects of EUVL technology. For example, the technology for fabricating defect free EUVL masks has been proven hard to develop. For the second route, both CNT and graphene are regarded as potential replacements for Si in the semiconductor integrated circuit industry. Research on carbon nanotubes (CNTs) started in the early 1990s [3], while research on graphene has already gone on for about 10 years [4]. However, scientists are still working on solving the chirality issue of CNTs [5] and the orienting and edge cutting issues of graphene [6]. Closely related to the feature size reduction, another serious problem arises. When the feature sizes on Si integrated circuits become smaller, the density of transistors per unit area increases tremendously. As a result, the power consumption and the heat generation of VLSI increase enormously and become prohibitive for further reducing the integration density. Researchers expect that the integration of III-V materials on Si can lead to smaller supplied voltage to transistors, which may reduce the power consumption and alleviate the heat generation [7].



**Figure 1.1** Band structure of (a) Gallium Arsenide; (b) Silicon [8]

As we pointed out previously, the bandgap structure is another limiting factor for silicon, especially in optoelectronics. Figure 1.1 shows the band structure of GaAs and Si. As we can see in figure 1.1, the  $\Gamma$  valley of GaAs is the lowest point of its conduction band, which is at the same position as the valence band peak in the momentum space. This means that the requirement for momentum conservation can be easily satisfied when the electrons in the conduction band edge recombine with the holes in the valence band edge to generate photons. Si is an indirect bandgap material. The lowest point in its conduction band is at a different location from the valence band peak in the momentum space. Because the momentum of a photon is zero, as compared to the momentum difference between the electron and the hole, radiative recombination of an electron and a hole in Si requires absorption or emission of a phonon to conserve momentum, which renders this process very inefficient. This is the obstacle that stops silicon from being widely used as an optoelectronic material [9]. A lot of effort and funds have been devoted to Si photonic research in order to develop a technology to manufacture Si semiconductor light sources. But these efforts have not yet achieved a satisfactory result. Thus, most optoelectronic devices are made of III-V compound semiconductor materials. The direct energy bandgap of ternary or quaternary III-V semiconductor materials can be engineered by controlling the composition of the III-V components. Although III-V compound semiconductors have more favorable optoelectronic properties than Si, their shortcomings are also obvious. III-V compound semiconductor materials are fragile, expensive and hard to process.

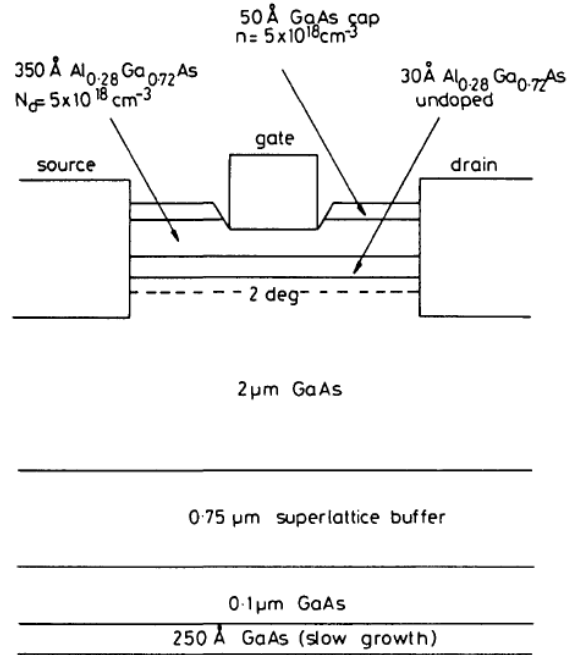
The idea of growing III-V compound semiconductor materials on Si substrates was proposed to overcome the limitations of both material platforms pointed out above. In electronics, such integration is a way to solve the silicon feature size limitation and the power consumption problems. Because the III-V semiconductor materials have better electron transport properties than silicon, the MOSFETs with channels made of III-V semiconductor materials have lower power consumption and higher switching speed than conventional silicon MOSFETs [10],[11], and silicon VLSI systems with high speed GaAs input and output circuits have higher throughput [12]. In addition, Si devices are cheaper and VLSI technology is based on Si. Therefore, the integration of III-V semiconductor materials and Si takes advantage of both the electronic properties of III-V materials and the matured CMOS technology. It may also be the most economically viable way to be compatible with the existing fabrication technology, which reduces the overall development cost as compared to switching to an entirely new material platform. On the other hand, in optoelectronics, most light sources and detectors are made of III-V semiconductor materials. The demand for ever increasing data transmission speed and the potential of using optical links to replace the metal interconnection in VLSI drive the need for optical device integration with silicon circuits. Even after decades of vigorous endeavors in silicon photonics, the fundamental physical limitations of using silicon as an optoelectronic material are still present. Therefore, the integration of III-V semiconductor materials and silicon is the most practical and promising way to fabricate monolithic optoelectronic devices, at least in the near future.



## 1.2 Invention and Development of III-V Semiconductor SAE on Si

Selective area epitaxy (SAE) is one of the fabrication methods that can potentially be used to monolithically manufacture III-V devices on silicon. SAE is a bottom-up process that typically uses dielectric masks on a semiconductor substrate to inhibit deposition on the masked region during the epitaxial growth. Epitaxial layers locally grow on the selected areas of substrate surfaces and form patterns defined by the dielectric masks. This section will introduce early works and developments of III-V SAE on silicon substrates.

The III-V on silicon growth technology started to be developed in the late 1970s. In the beginning, many attempts resulted in failures because some unsolvable problems existed at that time. For example, (1) in the growth process, if the surface of the Si is not perfectly cleaned, contaminants on the substrate, such as oxide and carbide, prevent layered growth and cause crystal defects [13]; (2) the lattice mismatch between GaAs and silicon is greater than 4%, which generates dislocations in the epitaxial layer and degrades the fabricated device; (3) the anti-domain disorder issue needed to be resolved for growing polar material on a nonpolar substrate; otherwise, the III-V on Si interface layer will have different electronic properties [14]. At that time, people were more familiar with the properties of III-V on III-V compound semiconductor growth. The unfamiliar process of III-V on silicon growth posed new fundamental difficulties to researchers [15]. Many theoretical investigations were carried out to address these problems. Combined with previous studies on heterogeneous crystal growth such as how to deal with lattice mismatch, scientists gradually mastered the technique to grow III-V semiconductor on silicon in the early 1980s.



**Figure 1.2** Cross-section view of the MODFET device made by Fischer in 1984 [15]

As an example of creating III-V on Si substrate devices, Uppal and Kroemer reported the growth of GaAs on Si (211) with MBE in 1984 [15]. They found that using Si substrates with the crystallographic (211) surface could avoid the polar on non-polar problem associated with III-V semiconductor on silicon growth. The detailed principle of this technology will be introduced in Chapter 2.

In the same year, Fischer at the University of Illinois successfully grew GaAs and AlGaAs directly on silicon (100) substrates and made monolithic MODFETs [16]. Figure 1.2 [15] shows the cross-sectional structure of the MODFET they made. The structure was grown on (100) oriented p-type silicon substrate with MBE. The fabricated GaAs/AlGaAs MODFETs had transconductance of 170 mS/mm at room temperature and exhibited no looping. This research proved that Si (100) substrate tilted by a few degrees could be well suited for GaAs/AlGaAs growth.

In 1989, Salerno published a paper on selective MOCVD growth of compound semiconductor on Si Substrates [12]. This was the first use of selective area epitaxy to grow III-V materials on Si substrate. The III-V materials that they used in their research were GaAs and alloys of GaAs, such as AlGaAs. The growth substrate was a single crystal Si (001) wafer. A layer of SiO<sub>2</sub> was used as the mask material. After photolithography and etching, the designed pattern was locally removed from the SiO<sub>2</sub>, so that the regions of the silicon surface where the researchers wanted to grow GaAs were exposed. The growth process was similar to the general III-V material growth, except that the epitaxial layers only grew on the exposed silicon surface [12].

Yamaguchi also published a paper [17] on GaAs selective area growth on Si substrates in 1989. In their research, they found selective area epitaxy reduced the residual stress and dislocation density in the grown GaAs layers. They developed a model to analyze this reduction based on the assumptions that the generation of dislocations was caused by thermal stress in the films and the dislocation density reduction was caused by stress relief [18]. In 1990, Yamaguchi claimed that as a result of the dislocation density reduction in III-V epitaxial layers in selective area epitaxy, GaAs-on-Si solar cells and red and yellow InGaP-on-Si LEDs were successfully fabricated [17].

In 1991, Karam found [19] that selective area epitaxy of GaAs on Si helped to eliminate wafer warpage, to reduce film cracking, and to reduce tensile stresses when the growth area was less than 200  $\mu\text{m}$ /side. When the area was below 10  $\mu\text{m}$ /side, complete stress relief was achieved after oxide removal. A thermal cycle growth technique was used in their process which resulted in reduction of the dislocation density by two orders of magnitude.

Driven by the motivation of fabricating blue to ultraviolet optoelectronic devices, researchers started to work on group III nitrides selective area growth on silicon in the early 1990s. Stevens reported the selective area growth of GaN and polycrystalline InGaN on Si (111) substrates with cyclotron resonance plasma-assisted MBE process in 1993 [20].

In the 1990s and early 2000s, scientists applied the III-V selective area growth technology to monolithic optoelectronic device fabrication. Before the 1990s, photodiodes and their silicon readout circuitry were separated in photodetectors. The interconnection was normally made by wire or indium bump bonds. Before high quality selective area growth of III-V on silicon substrates solving the epitaxial layer dislocation problem [21], typical III-V on Si growth failed to produce high quality epitaxial layers for monolithic device fabrication. The lattice mismatch at the growth interface would result in dislocations which cause sufficient leakage current to degrade the performance of photodiodes. In 1995, Joshi et al. developed the method and the apparatus for monolithic optoelectronic integrated circuit using selective epitaxy of III-V material on silicon substrate [21]. In his experiment, Joshi grew a photodiode on a silicon substrate using InGaAs with selective area epitaxy technology.

In 2000, Yang et al. reported the fabrication and characterization of blue GaN-InGaN multi-quantum well LEDs on (111) Si substrates. The selective area growth was carried out in both MBE and low-pressure MOCVD [22]. In 2001, self-assembled InAs quantum dots were selectively grown on Si substrates by Choi et al. [23].

From the mid-2000s, scientists started to directly pattern III-V nano-scale structures on Si by selective area growth. In 2008, researchers reported direct integration of III-V compound semiconductor nanostructures on Si by selective area epitaxy [24]. In this research, they

patterned GaAs nanoholes and nanowire trenches on Si (111) substrates. In the same year, scientists achieved selectively grown GaN nanocolumns on Si (111) substrates with titanium growth masks [25]. In 2011, Alsubaie et al. demonstrated the selective area growth of hexagonal and rectangular shaped GaAs crystals on Si substrates [26].

In conclusion, III-V compound semiconductor epitaxy on Si substrates technology started to develop from the late 1970s. It went through a rapid period of development during the early 1980s and many III-V on silicon devices were fabricated in the laboratory in the mid-1980s. As the technology further advanced, researchers started to utilize dielectric masks in the III-V material on Si substrate growth process in order to directly define the structures of their devices during the growth process in 1987. In contrast to the top-down processes, selective area epitaxy of III-V compound semiconductor material on Si substrates is a bottom-up process that is able to grow higher quality epitaxial layers and allows easier fabrication of both GaAs and Si devices on the same Si substrate. With these advantages, selective area epitaxy of III-V materials on Si substrates is highly desirable [12]. After more than 20 years' development, this technology reached the stage of growing high quality III-V nano-scale patterns on Si for the applications in optoelectronics. The monolithic integration of optoelectronic devices and complementary-metal-oxide-semiconductor (CMOS) Si circuits has great potential of becoming a critical technique for the next generation high-speed communication and computing systems. In the next chapter, we will discuss the detailed growth technique of III-V on Si SAE and the issues and the solutions of the technology.

## 2. GROWTH TECHNIQUES AND OPTIMIZATION

### 2.1 Typical Growth Techniques for III-V SAE on Si with MOCVD

Both MOCVD and MBE are used in research on selective area epitaxy of III-V materials on Si substrates. Many growth processes were developed by different research groups. These growth processes are largely similar but differ in details to fulfill the requirements of each individual research. We are going to introduce the typical growth processes for both MOCVD and MBE. There are issues associated with these typical processes, which prevent the growth of high quality epitaxial layers. These issues will be discussed later in this chapter and possible solutions will also be provided.

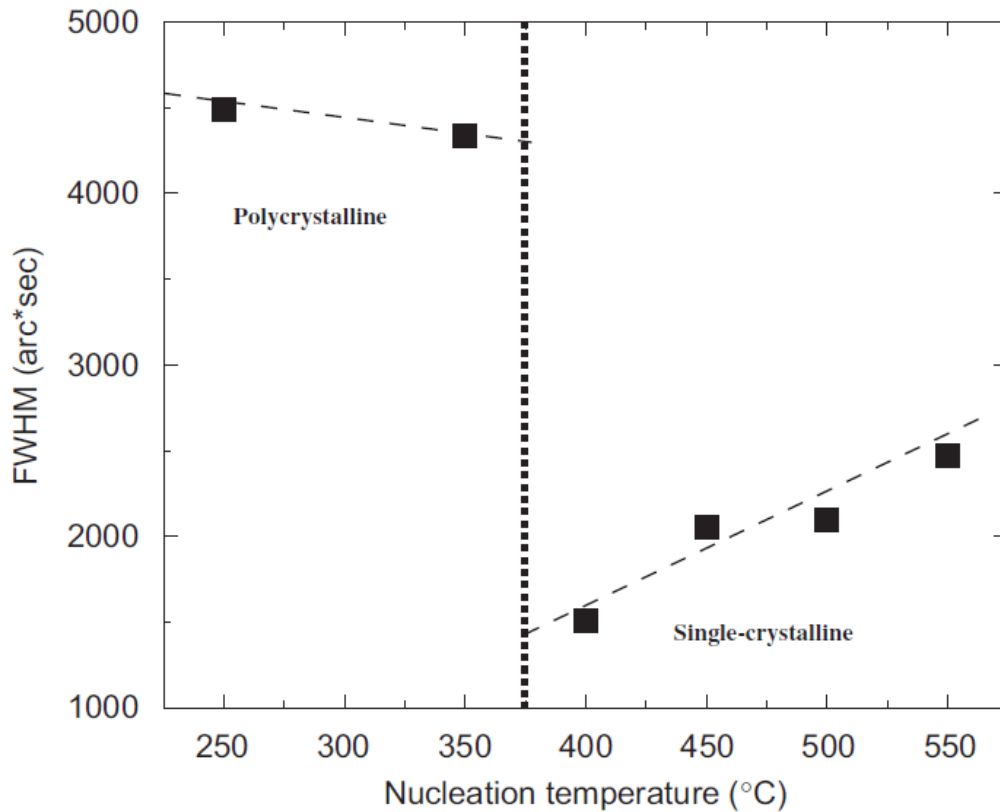
The typical recipe used in selectively area growth of compound semiconductor materials on Si substrates using MOCVD can be found in Salerno's patent [12]. At first, a silicon substrate with specific crystallographic orientation is chosen. This silicon wafer can be a virgin wafer or a wafer with prefabricated structures on it. Once the proper wafer is obtained, a mask layer is deposited on the wafer surface. There are various choices of the dielectric materials that may serve as the growth mask. The most popular ones are  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$  deposited with CVD [27],[28],[29]. In Salerno's procedures, his group used 0.2  $\mu\text{m}$  of CVD deposited  $\text{SiO}_2$  as the dielectric mask. The next step is to define the selective growth patterns using standard photolithography. It involves coating the  $\text{SiO}_2$  mask with photoresist (PR), defining the desired growth pattern on the photoresist and exposing it under UV light. After the PR is fully developed and washed away, the PR left on the wafer surface serves as the etching mask to selectively remove the  $\text{SiO}_2$  from the Si wafer surface with a hydrofluoric acid solution (1 HF :

1H<sub>2</sub>O); then the PR is striped off in acetone. The Si wafer with the patterned SiO<sub>2</sub> mask on top of it is thus ready for further growth.

Before loading to the MOCVD growth chamber, the Si wafer with growth mask needs to be perfectly cleaned to remove all impurities from the surface of the SiO<sub>2</sub> mask. This cleaning step is crucial in the fabrication process because the remaining contaminants, especially metallic contaminants, may nucleate and form polycrystalline GaAs on the surface of the dielectric mask, which is undesirable for high quality selective area epitaxial growth. These residual contaminations may also interfere with the growth of GaAs at the openings of the SiO<sub>2</sub> mask on the Si substrate. Research showed that the surface metal contaminants can be suppressed to negligible levels by proper chemical treatments [30],[31]. Various chemical solutions can be used. In the example given in Salerno's patent, the solution is 1H<sub>2</sub>SO<sub>4</sub> : 1H<sub>2</sub>O<sub>2</sub>. Then, the wafer is immersed in DI water to wash off the solution. The next step is to remove the residual oxide on the exposed Si surface at the SiO<sub>2</sub> mask openings. The residual oxide is generated during the fabrication process when the wafer is exposed to air. The residual oxide left on the openings of the Si surface will result in non-epitaxial GaAs growth on the Si substrate. In Salerno's research, he used the solution 1HF : 1H<sub>2</sub>O<sub>2</sub>. Then, the wafer is rinsed in water again and dried with N<sub>2</sub>.

Finally, the wafer is loaded into the MOCVD growth chamber to finish the selective area growth. This loading process should be performed right after the residual oxide removing to prevent it from oxidizing again. After loading the wafer in, the growth chamber must be purged with N<sub>2</sub>, H<sub>2</sub> or evacuated to prevent oxidation and contamination. Then, the chamber needs to be pumped down and purged with H<sub>2</sub> to obtain a pure H<sub>2</sub> growth environment. The two-step

growth method was widely used in research. Salerno's group used low pressure MOCVD growth in their process. The pressure in the growth chamber during the selective area growth needs to be controlled to a certain pressure between 10 and 100 Torr. In their process, they chose 100 Torr. Then, the patterned wafer is heated from room temperature to 775 °C in order to clean the Si surface at high temperature. This is the last step for cleaning of the Si surface, and it also functions as the stimulation for the atomic arrangement reconstruction on the substrate surface which facilitates high quality GaAs growth. Then, GaAs is grown on the patterned Si substrate by the a two-step growth process [32],[33]. The first step is the nucleation of GaAs on Si substrate at low temperature. Figure 2.1 [26] shows temperature dependence of the full-width-half-maximum (FWHM) for 200 nm thick GaAs films grown on Si measured by



**Figure 2.1** X-ray diffraction measured full-width-half-maximum for 200-nm thick GaAs films growth on Si as a function of nucleation temperature [26].



X-ray diffraction. From the X-ray diffraction results, we see that the FWHM of single-crystalline is much lower than poly-crystalline as shown in Figure 2.1, which indicates that the single-crystalline lattice is more uniform than the poly-crystalline one. Based on this result, the nucleation process should be accomplished above and close to 375 °C in order to achieve high quality single-crystalline epitaxial growth. In Salerno's research, the wafer is cooled down to approximately 420 °C to initiate the first nucleation layer of GaAs. The nucleation layer of GaAs is selectively deposited on the exposed surface of the Si substrate, while no deposition on the dielectric mask should take place. This process is continued until all the exposed Si surfaces are covered. Then, in the second step, the temperature rises to between 600 °C and 700 °C to reach the typical growth rate of GaAs. All the other conditions are set to the conventional conditions used for normal epitaxial GaAs growth.

We have shown the typical selective area epitaxy process to grow III-V compound semiconductor materials on Si substrates using MOCVD. This process may be adjusted to achieve better growth results for specific application. We will cover these adjustments when we discuss specific applications in later sections.

## **2.2 Typical Growth Techniques for III-V SAE on Si with MBE**

In this section, we are going to show the detailed process of MBE selective area epitaxy of III-V semiconductor materials on Si substrates [34],[35],[36]. We will use the process developed by Lee et al. as an example [34],[36]. In their research, a heavily n doped Si (001) surface tilted 3.5° towards <110> axis is chosen as the substrate to grow on. First, the wafer is cleaned repeatedly in 5H<sub>2</sub>SO<sub>4</sub> : 1H<sub>2</sub>O<sub>2</sub>. Then, an 800 Å thick SiN layer is deposited on the Si surface by CVD as the growth mask. The wafer is patterned by photolithography and etched with reactive

ion etching (RIE) with the fully developed PR as etching mask. The etching is done by the mixture of  $\text{CHF}_3$  and  $\text{O}_2$  with 20% over-etch time to ensure the SiN in the defined area is completely removed.

The second procedure is cleaning. In this procedure, the usual wafer preparation steps for MBE are applied to the Si wafer [13]. The cleaning process has two steps, chemical treatment and high temperature cleaning. In chemical treatment, the patterned Si wafer is treated by chemical processes which include degreasing, elimination of the contaminants on the Si substrate, and forming a layer of passivated oxide on the Si surface. The full process and chemicals used can be found in Ishizaka's report [13]. The repetition in the  $\text{HNO}_3$  boiling procedure is to repeatedly etch the oxidized layers, which eliminates the carbon and other active contaminants in the growth procedure. After the chemical treatment, the wafer is loaded into the MBE growth chamber and heated to between 680 °C and 930 °C for 5 to 10 min in ultra-high vacuum to finish the final cleaning procedure.

Similar to the MOCVD process, a two-step growth method is applied to the growth. The temperature in the chamber is reduced to 400 °C in order to initiate the growth. The molecular beam Ga source is flowed into the chamber to deposit approximately one monolayer of Ga. The  $\text{As}_2$  vapor generated by thermal decomposition of GaAs is used as the As source [12]. The  $\text{As}_2$  source is heated and flowed in to the chamber after the formation of the first monolayer of Ga to form the first monolayer of GaAs [37]. After the nucleation is completed, the Ga and  $\text{As}_2$  sources are both flowed in to continue the growth. The growth temperature is raised to 570 °C to increase the growth rate until the growth process completes.

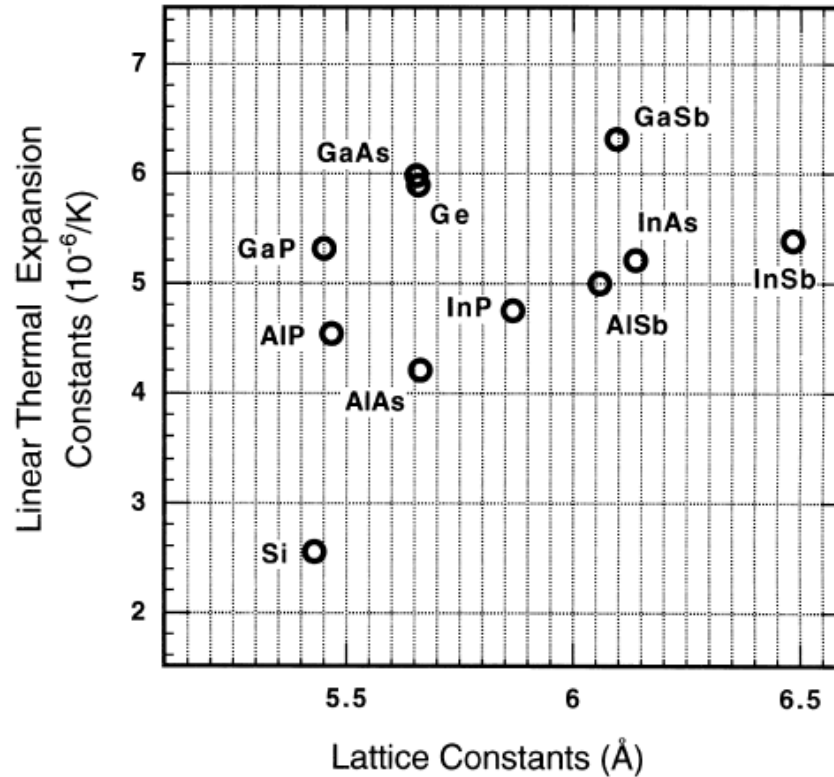
The detailed growth procedures introduced in this section are summarized from various growth procedures developed by different research groups. These procedures are good examples to follow, but issues and challenges exist, which will be discussed in the next section.

## 2.3 Issues with Existing Technology and Solutions

Many problems and challenges exist in the process of III-V compound semiconductor material growth on Si substrates such as growing of polar materials on non-polar materials, large lattice mismatch between III-V materials and Si, large thermal expansion mismatch between III-V and Si, highly stressed growth layers, anti-phase domain disorder, poor surface morphologies and auto doping of Si from substrate into the grown layer [31]. In this section, we will focus on the main issues associated with growing III-V material on Si substrates and solutions to those issues, which are dislocation and anti-phase domain disorder.

### 2.3.1 Dislocation

Dislocation is one of the primary sources of defects found in the epitaxially grown III-V films on Si substrate. Several factors contribute to the dislocation near the interface between the III-V crystal and the Si substrate, which mainly include the lattice mismatch and the thermal expansion parameter mismatch. Researchers found that even with the widely used two-step growth method introduced in section 2.1, the dislocation densities in the III-V films grown on Si substrate were as high as  $10^8 - 10^9 \text{ cm}^{-2}$  [31], which is much higher than the standard dislocation density  $10^4 - 10^5 \text{ cm}^{-2}$  in III-V epitaxial layers.



**Figure 2.2** Thermal expansion parameters of III-V and elemental materials vs. their lattice constants

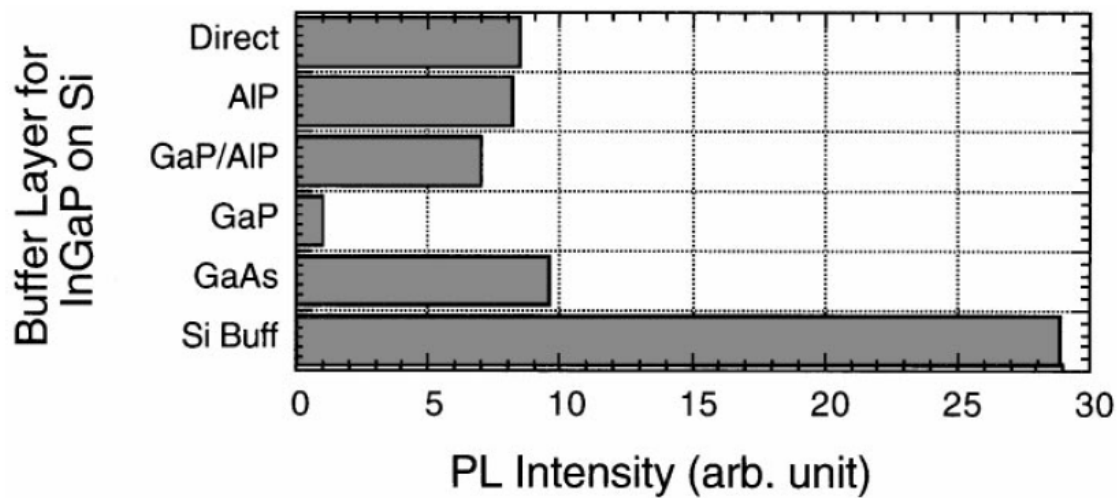
Figure 2.2 [31] shows the different thermal expansion parameters of III-V materials and Si vs. their lattice constant. We can see that the difference between the linear thermal expansion constants of III-V materials and that of Si is big. In addition, except for GaP and AlP, the lattice mismatch between the III-V materials and Si is large, too. For example, Si and GaAs have 4% mismatch between their lattice constants as Figure 2.2 shows, which generates lattice strain in the grown GaAs layers, and results in dislocations in the epitaxial layers. The dislocations caused by the thermal expansion parameter difference are generated during the cooling process at the end of growth. When the III-V on Si growth is finished, the growth chamber and the wafer need to be cooled down in order to unload. In this process, when the temperature drops, the lattice changes caused by the thermal expansion are different between the GaAs epitaxial layer and the Si substrate [31]. This dislocation generation mechanism during the

cooling stage of growth was reported by Tachikawa and Mori in 1990 [38]. In their experiment, they found the GaAs and GaP layers they grew on Si substrates had high quality if they stayed at the growth temperature at 650°C. The dislocation density measured at the growth stage was only about  $10^4 \text{ cm}^{-2}$ . However, when the cool-down process was finished after the growth, the dislocation density increased to  $10^6 - 10^7 \text{ cm}^{-2}$ . In the same experiment, they showed that although the lattice mismatch between GaAs and Si was 4% while that between GaP and Si was only 0.4%, the 10 order difference in lattice mismatch did not generate much difference in the dislocation density. Based on this result, Tachikawa and Mori suggested the dislocations in III-V on Si growth were mainly generated by thermal expansion mismatch.

Many methods were developed trying to solve the dislocation issue of III-V on Si substrate growth. We are going to introduce three of them: substrate surface preparation, initial buffer layer and intermediate layer growth and low temperature growth [31].

Substrate surface preparation before loading into the growth chamber is a crucial step. The contaminants on substrate surfaces such as oxide, carbide and metallic contaminants prevent growth or generate polycrystalline growth on substrates, which is one of the main causes of dislocation generation in III-V semiconductor material on Si growth [13]. In 1996, Kawanami et al. tested the dislocation generation by unclean Si substrates [39]. In their experiment, they grew  $\text{In}_x\text{Ga}_{1-x}\text{P}$  films on Si substrate with MBE. Instead of directly growing  $\text{In}_x\text{Ga}_{1-x}\text{P}$  layers on top of Si substrate, they grew buffer layers between the substrate and the epitaxial layers. As Figure 2.3 [39] shows, they used  $\text{In}_x\text{Ga}_{1-x}\text{P}$  (direct growth without buffer layer), GaP, AlP and GaAs as the buffer layer, and finally they tried the same thickness of Si as the buffer layer. The photoluminescence (PL) intensities indicate the quality of the grown films,

where the film with fewer dislocations generates higher PL intensity. We can see that the growth with the Si buffer layer, which intuitively should not increase the quality of the grown film, had at least three times higher PL intensity than the others. Further research showed that the growth of the Si buffer layer between the silicon substrate and the epitaxial layer covered the contaminants on the substrate surface and resulted in higher quality III-V epitaxial film grown on top. This experiment proved the importance of the substrate cleanness in dislocation reduction in the SAE growth.



**Figure 2.3** The PL intensity obtained from  $\text{In}_x\text{Ga}_{1-x}\text{P}$  on silicon growth samples with different buffer layers

Ishizaka and Shiraki developed the cleaning method that was widely used by research groups for growing III-V on Si substrates [13]. As introduced in section 2.1, this cleaning method first uses chemical treatments to generate an oxidized layer on top of a Si substrate, and this oxidized layer which contains the contaminants is etched down. Then a very thin oxide layer is formed on the substrate surface to protect the Si surface during the loading process. The second cleaning process is that after the wafer is loaded into the growth chamber, a 900 °C

thermal etching is performed to remove the thin oxide film. Thus, the atomically clean surface is obtained [13].

The second method to reduce the dislocation density in III-V on Si growth is the initial buffer layer and the intermediate layer growth. The purpose of using buffer layers is to engineer the lattice constants of the growth substrate to match the lattice constants of the III-V epitaxial layers. For example, because the lattice constant of Ge is close to that of GaAs, the 4% lattice mismatch between Si and GaAs can be reduced gradually by a graded  $\text{Si}_x\text{Ge}_{1-x}$  buffer layer between Si substrate and GaAs epitaxial layer with 100% Si at the Si substrate interface and 100% Ge at GaAs epitaxial layer interface [40]. Many different buffer layers were already examined by various research groups. It was shown that the buffer layers made of ZnSe [41][42], GaSe [43] and GaSb [44] were softer than GaAs and Si. The softer buffer layers were used in these researches, because the dislocations were more likely to exist in soft layers than in hard layers. The soft buffer layers could sustain most of the strain caused by the lattice mismatch and stop the mismatch propagating into the GaAs epitaxial film [31]. GaP based buffer layers were also developed, since GaP had a lattice constant between Si and GaAs. With GaP based buffer layers, dislocation density in GaAs epitaxial films was reduced to  $3 \times 10^6 \text{ cm}^{-2}$  [45]. Intermediate layers such as strained layer superlattice (SLS) grown between epitaxial layers and Si substrates were also widely used in the III-V on Si growth technology. The dislocations in the epitaxial layers were expected to bend into the strained interfaces of the intermediate layer to promote dislocation interactions [31]. In one research, Uchida et al. reported the effect of dislocation reduction using strained InGaAs intermediate layers in GaAs grown on Si (001) [46]. Both the In content and the strain effect caused by the InGaAs intermediate layer can reduce

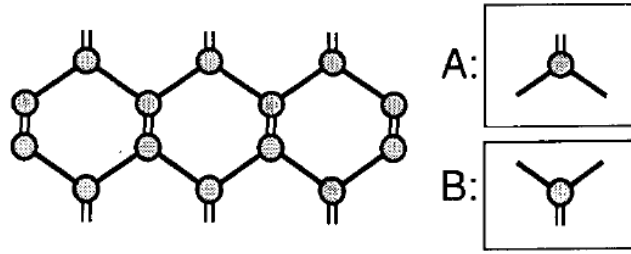
dislocation density in the GaAs epitaxial layer. Uchida's study showed the correlation between these two effects and the dislocation density. The best quality layer they achieved had a dislocation density of  $8 \times 10^6 \text{ cm}^{-2}$ .

The third method to reduce dislocation in III-V films grown on Si substrate is low temperature growth. As introduced previously, the thermal expansion parameter mismatch between GaAs and Si is 63% [40]. During the cooling stage after the growth process finishes, many dislocations are generated in the III-V epitaxial layers because of the thermal expansion parameter mismatch. The low temperature growth method of III-V material on Si substrate reduces temperature variation at the cooling stage of growth. This method is expected to largely reduce the effect of thermal expansion parameter mismatch. As an example, Shimomura et al. grew GaAs on Si substrates at 330 °C with MBE, and they successfully reduced the dislocation density to  $7 \times 10^4 \text{ cm}^{-2}$  [47],[48]. However, reports also show that the low temperature growth may introduce other problems such as point defects to the epitaxial layers [31].

### 2.3.2 Anti-phase domain disorder

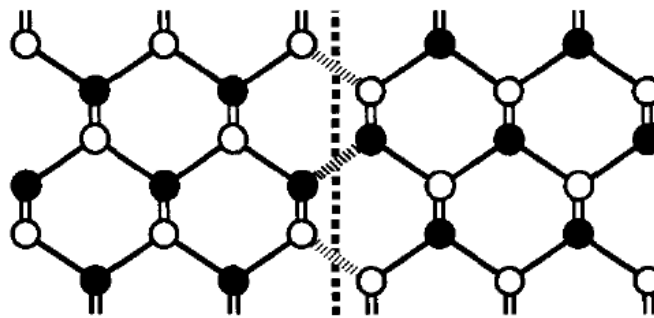
Another issue of III-V on Si substrate growth is called anti-phase domain disorder. Anti-phase domain disorder is caused by polar material on non-polar material growth. There are two interpenetrating sublattices in a Si diamond crystal structure. As Figure 2.4 [14] shows, the type A atoms belong to one sublattice, and the type B atoms belong to the other sublattice.





**Figure 2.4** Two types of sublattice in silicon crystal

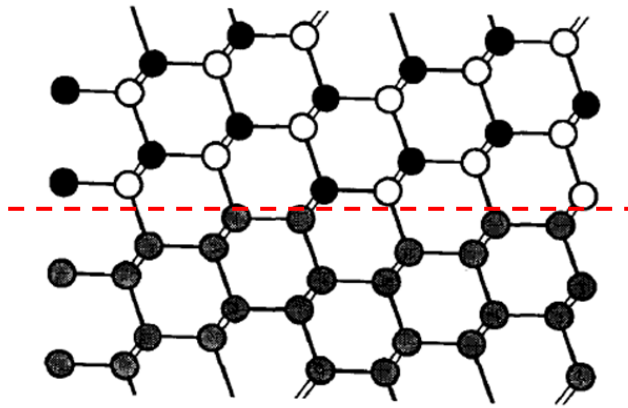
For Si, all the locations in both sublattices are occupied by Si atoms. However, for III-V materials such as GaAs, each of the two sublattices needs to be occupied by different species of atoms, so that the adjacent atoms are always different [14]. In the growth interface between the III-V material and the Si substrate, the order of the atoms can be switched if no special technology is applied, which changes the electronic property of the epitaxial layers. In further study, researchers found that on Si substrate surfaces, if there is a step which has the height of odd multiples of atomic layers, the sublattice occupancy will be reversed. As a result, along a step which has the height of odd multiples of atomic layers, the same species atoms in III-V materials



**Figure 2.5** III-V growth on Si surface with a step which has the height of odd multiples of atomic layers

will be bonded to each other as shown in Figure 2.5 [14]. This issue does not exist in steps which have the height of even multiples of atomic layers. However, on (100) Si surfaces, the most common step height is one atomic layer.

Three known solutions can be used to solve the anti-phase domain disorder issue. The first one was found by Kroemer et al. [14]. They found that the GaAs grown on (211) oriented Si had no anti-phase domain disorder on the III-V side of the growth interface. The GaAs on (211) Si cross section is shown in Figure 2.6 [14]. Above the red line, the



**Figure 2.6** Cross section of GaAs grown on (211) Si surface

black atoms are As atoms and the white atoms are Ga atoms. The gray atoms below the red line are Si atoms. The cross section figure shows that there are two kinds of sites on the (211) Si surface. One is a double bonding site, and the other is a single bonding site. These two types of sites exist on the growth surface alternately. Compared with Ga atoms, As atoms have higher tendency to bond to Si atoms. During the growth, As atoms will bond to the stronger double bonding site and leave the single bonding site to Ga atoms. Therefore, the use of (211)

Si solves the anti-phase domain disorder issue [14]. The detailed growth process is provided in [15]. Uppal and Kroemer believed that the (211) orientation allows the growth of the high quality GaAs layers on Si substrate.

However, most researchers still prefer to work on the conventional (100) orientation Si substrates. In 1986, the substrate thermal annealing method was invented by Sakamoto and Hashiguchi [49]. In their research, they found that if (100) Si substrates were annealed 20 min under the temperature 1000 °C, all the single atomic layer height steps on the Si surface would be transferred to double atomic layer height steps. Since anti-phase domain disorder does not happen at double atomic layer height steps, this thermal annealing method solves the anti-phase domain disorder issue.

The last solution to the anti-phase domain disorder problem was reported in the paper of Fischer et al. [50],[51]. In the growth process of GaAs on their (100) Si substrate, the researchers tilted the substrate by a few degrees towards the (011) plane. The misorientation of the substrate decreased the number of the single atom high steps and increased the number of double atom high steps on the growth surface. The work of Fischer et al. confirmed the absence of anti-phase domain disorder [14] using the tilted substrate.

In conclusion, the common issues that exist in the III-V material on Si growth technology such as lattice mismatch, thermal expansion parameter mismatch and anti-phase domain disorder are introduced in this chapter. The methods developed by different research groups to solve these issues are also presented. Some of these solutions also have their own limitations. Research is still needed in this area to achieve even higher quality growth. There are many other issues with some specific structure growth processes. In the next chapter, examples of

monolithically fabricated III-V on Si devices and structures will be introduced. A few specific issues and solutions will be presented with the examples.

### 3. MONOLITHIC DEVICE AND STRUCTURE FABRICATION EXAMPLES

Monolithic III-V semiconductor device fabrication on Si substrates has been a popular topic since the 1980s [33],[52],[53],[54]. The high electron mobility and direct bandgap of III-V materials made them preferable to Si in optoelectronics applications and in high speed electronic devices. Integration of III-V devices on Si substrate provides a solution to build compatible optoelectronics and high speed devices together with Si based CMOS circuit. There are many applications with big potential which require the integration of III-V optoelectronic devices and quantum confined structures on Si [55]. In this chapter, we will use three examples, namely the LEDs, the quantum dots and the nanowires, to illustrate how to fabricate III-V devices on Si substrate using selective area epitaxy.

#### 3.1 Light Emitting Diodes

The low cost of Si substrate and the potential of integrating III-V LED and Si ICs drives the development of LED on Si fabrication technology [22]. The growth of device quality III-V epitaxial layers on Si substrates is required for monolithic LED fabrication. The defects caused by lattice mismatch would significantly decrease the lifetime of light emitting devices [22]. Two LED examples will be shown in this section. The first example we show used a GaN-InGaN based structure to eliminate the effect of defects on the device lifetime. Previous research has shown that the GaN-InGaN based LEDs on sapphire substrates have a lifetime longer than  $10^4$  hours, although the devices have about  $10^8 - 10^{10}$  dislocations per  $\text{cm}^2$  [56]. Based on this information, Yang et al. designed the GaN-InGaN multi-quantum well LED structure on Si substrates [22].

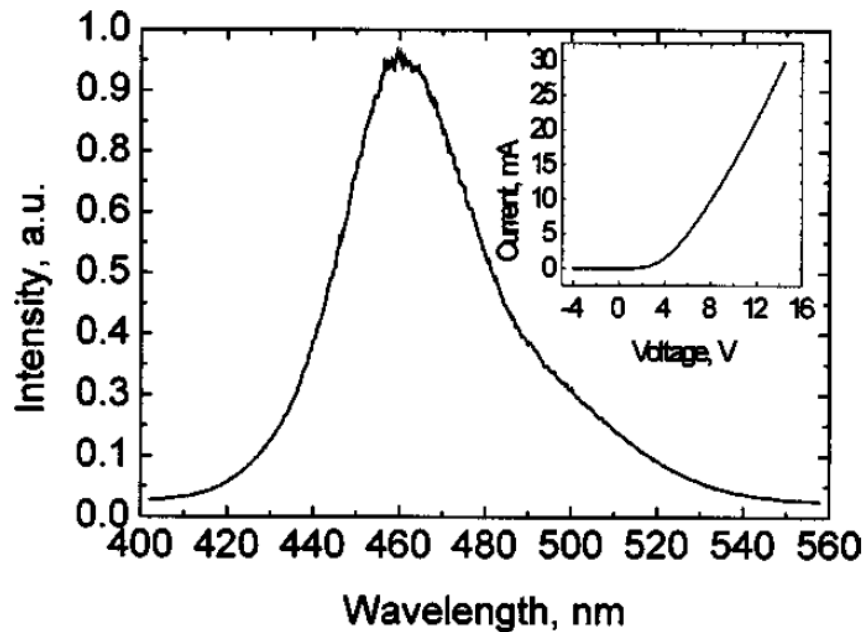
This device used AlN and  $n^+$  GaN as the buffer layer between the Si substrate and the multi-quantum well structure. The AlN buffer layer was a high quality single crystal layer grown

by MBE. The 100 Å thick buffer layer was grown at 800 °C on the (111) Si substrate. At first, a monolayer of Al was deposited on the Si surface by MBE. Then, the surface was exposed to NH<sub>3</sub> for several seconds to nucleate the AlN growth. After that, the rest of the AlN layer was deposited at the rate of 0.3 monolayers per second. Once the AlN layer growth finished, the sample was transferred to a LP-MOCVD chamber to grow the GaN and InGaN layers. A 0.2 µm thick n<sup>+</sup> GaN layer was grown on top of the AlN as the second buffer layer. This GaN layer was 1×10<sup>8</sup> cm<sup>-3</sup> Si doped. The growth was carried out with the flow of Triethylgallium and NH<sub>3</sub> at 900 °C and 76 Torr. When the buffer layer growth finished, a 0.2 µm thick SiO<sub>2</sub> layer was deposited on top, and a 300 µm × 300 µm square region was opened up with wet etching as the selective growth region. Then, in the defined region, the p-i-n LED structure was selectively grown by LP-MOCVD. The 500 Å thick 5×10<sup>17</sup> cm<sup>-3</sup> n type GaN layer was on top of the GaN buffer layer. Then the GaN-InGaN multi-quantum well layers with four In<sub>0.22</sub>Ga<sub>0.78</sub>N 30 Å thick quantum wells surrounded by 30 Å thick GaN barriers were grown on top. The 5×10<sup>17</sup> cm<sup>-3</sup> p type and 0.15 µm thick GaN layer was then deposited on top of the multi-quantum well layers. Finally, the n and p metal contacts were fabricated on the top of the n type Si substrate and the p type GaN cap layer respectively.

Figure 3.1 [22] shows the emission spectrum of the LED biased at 20 mA. The peak emission of this blue LED was at 465 nm. The full width at half maximum (FWHM) of the spectrum is 40 nm. The inset of figure 3.1 shows the output current vs. bias voltage curve of the LED. It had an onset voltage of 3.2 V and a forward differential resistance of 250 Ω.

The fabrication process of this GaN-InGaN multi-quantum well LED utilized a unique combination of MBE and LPMOCVD selective area epitaxy, which increased the quality of the

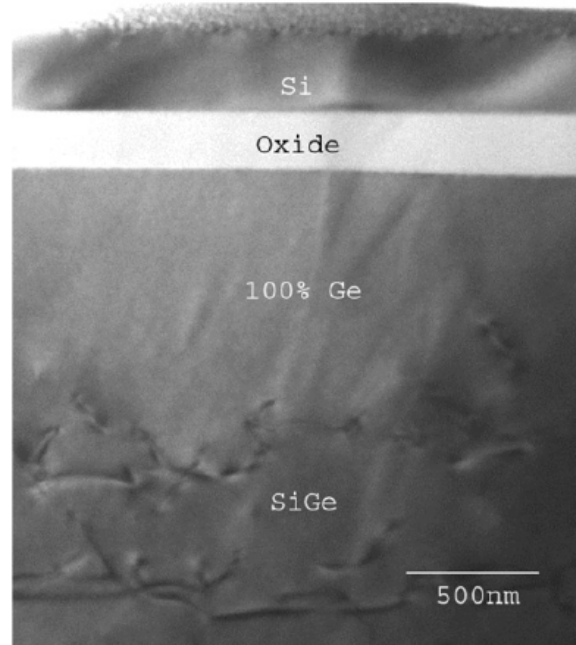
epitaxial layers. The growth also used the AlN and GaN buffer layers between the Si substrate and the multi-quantum well LED structure, which reduced the lattice mismatch between the junctions and also decreased the dislocation density. The successfully fabricated LED device was able to work between 0 and 250 °C. This selective area epitaxy fabrication of III-V LEDs simplified the fabrication process, grew lower dislocation epitaxial structures and also opened up the possibility of sequential growth for LEDs with multicolor pixels that integrated with Si circuit.



**Figure 3.1** Emission spectrum and output current vs. bias voltage curve of the GaN-InGaN multi-quantum well LED

In the second example of monolithic III-V LED device on Si substrates, we will show a more thorough study in the compatibility of III-V devices and Si CMOS circuits. The structure design and the fabrication process laid out a practical approach to integrate optoelectronic devices with CMOS circuits.

As one of the methods introduced to decrease the dislocation density, the use of a graded SiGe buffer layer between GaAs III-V epitaxial films and Si substrates was discussed in Chapter 2. However, researchers found a problem with this method in practice. The buffer layer caused about 10  $\mu\text{m}$  height difference between the III-V optoelectronic devices and the CMOS circuits. This resulted in complications for processing and difficulties in interconnections [55],[57],[58]. Therefore, Chilukuri et al. utilized the silicon on lattice-engineered substrate (SOLES) platform and developed the process that successfully fabricated the LED array at the same height with the silicon CMOS circuit without compromising both the III-V and the Si parts of the device [55].



**Figure 3.2** Cross-sectional TEM image of the SOLES wafer

Shown in Figure 3.2 is the structure of the SOLES platform. The first step of fabricating this device was growing the graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer on the (001) Si substrate. The composition of this buffer layer was changed gradually from pure Si to pure Ge. The growth was carried out in an ultra-high vacuum chemical vapor deposition system. The growth pressure was about 25

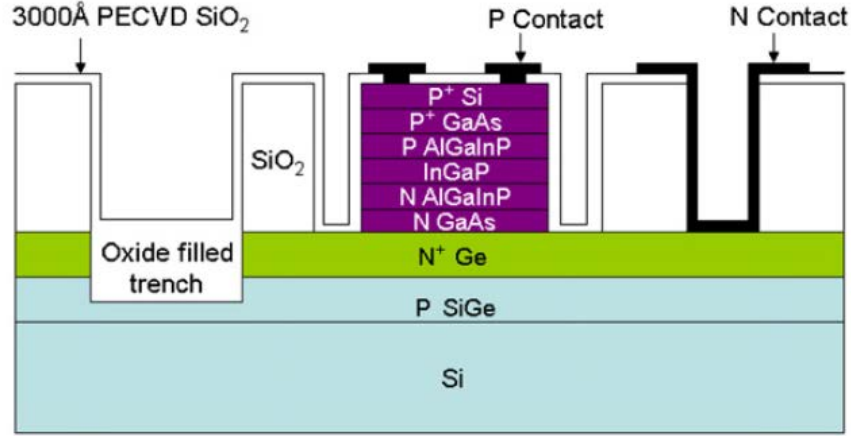


mTorr. The thickness of this graded layer was 10  $\mu\text{m}$ . The top part of this graded layer was a 100% Ge film. The  $\text{Si}_x\text{Ge}_{1-x}$  graded layer was p-doped with boron to  $5 \times 10^{17} \text{ cm}^{-3}$  and the Ge cap layer was n-doped to  $1.5 \times 10^{18} \text{ cm}^{-3}$  with phosphorous in order to make contact to the later fabricated III-V LED from the Ge region. After the growth, another Si wafer was prepared to transfer onto the top of the GeSi graded wafer. The transfer process was based on the SMARTCUT procedures [59]. The Si and GeSi graded wafer were both cleaned and oxidized to form flat and low roughness oxide surfaces. The two oxide surfaces were combined and annealed to form the structure shown in Figure 3.2. The SOLES fabrication procedures are shown in Figure 3.3.



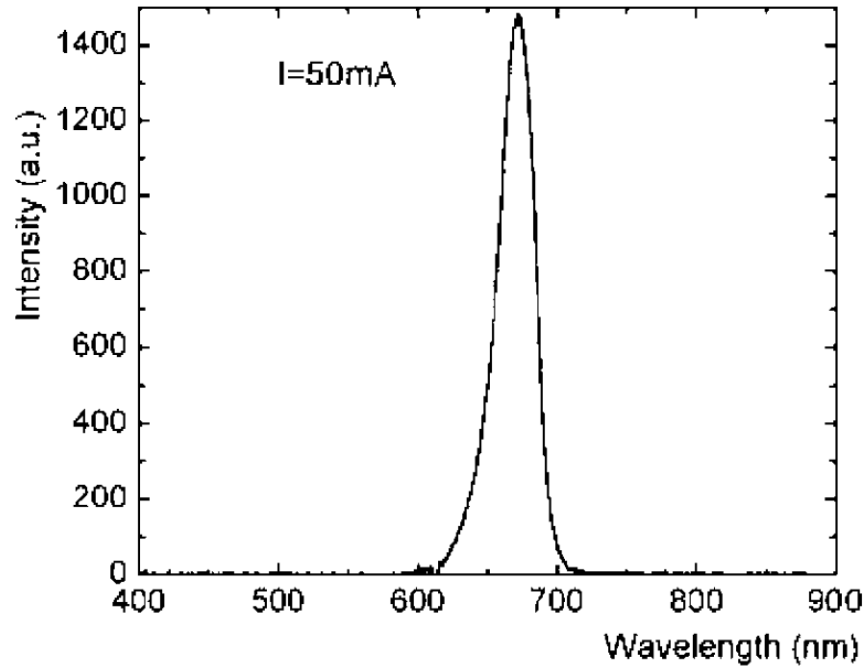
**Figure 3.3** Fabrication process of the SOLES platform

The fabrication of the LED started when the SOLES wafer preparation was finished. The silicon and the oxide layers in the defined LED area were etched to expose the lattice engineered Ge layer for GaAs growth.  $\text{SiO}_2$  mask layer was deposited and patterned to selectively grow the LED at defined region. Then, an n-type GaAs layer, n-type AlGaInP



**Figure 3.4** Cross section schematic view of the LED region on the SOLES wafer

barrier layer, InGaP quantum well layer, p-type AlGaInP barrier layer, p-type GaAs current spreading layer and p-type Si encapsulation layer were selectively grown by MOCVD at 650 °C and 100 Torr. The barrier layers were 200 nm thick and the quantum well layer was 220 Å. The p-GaAs current spreading layer was 50 nm thick and doped at  $1 \times 10^{19} \text{ cm}^{-3}$ . The Si encapsulation layer was 80 nm thick at the doping of  $1 \times 10^{21} \text{ cm}^{-3}$  for the p-type contact. The n contact was accessed by etching down and contact on the n-type Ge layer. Figure 3.4 shows the schematic of the cross section of the LED region on the SOLES wafer. The detailed step by step procedures and processing parameters can be found in the report of Chilukuri et al. [55].



**Figure 3.5** Output intensity vs. wavelength of the LED biased at 50 mA

Figure 3.5 [55] shows the spectrum of the SOLES based AlGaInP LED biased at 50 mA. The peak wavelength of this red LED was at 671 nm and the full width at half maximum was 30 nm.

With the SOLES technology, the optoelectronic devices can be fabricated at the same height with a device quality Si layer, which can be used for further processing of the CMOS circuit. The p-type Si encapsulation layer on top of the LED prevented contamination and damage of the optoelectronic device in the processing of the CMOS circuit afterwards. The high quality III-V layers growth on the Ge buffered Si substrate provided one solution for fabricating optoelectronic devices on selected area of SOLES wafers without damaging the remaining areas that can be used for CMOS circuits. The CMOS compatible AlGaInP visible LED arrays on the SOLES substrate were demonstrated in their experiment.

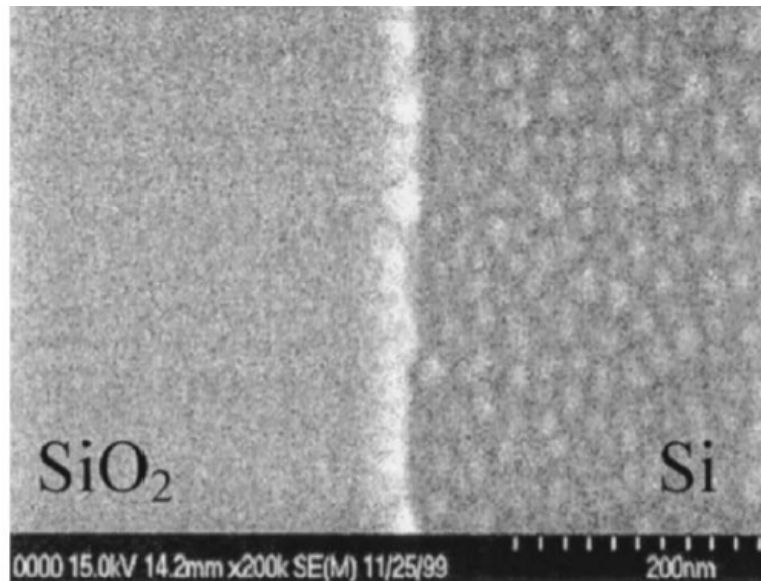
### 3.2 Quantum Dots

III-V quantum dot growth on Si substrate is a technology that opens up the possibility to integrate quantum dot devices with Si circuits. The Stranski-Krastanov self-assembled growth method has long been used in the quantum dot growth on III-V substrates [60],[61]. The Stranski-Krastanov quantum dots are formed as a result of relaxation of the strain caused by lattice mismatch between the epitaxial layer and the substrate. In the late 1990s, Shama et al. reported the growth of InAs quantum dots on Si substrate and Zhakov et al. studied the optical properties of those quantum dots [62],[63],[23]. Choi et al. started the selective area growth of InAs self-assembled quantum dots on SiO<sub>2</sub> masked Si substrate. The selective growth of patterned quantum dots on the defined areas on Si surface was done without lithography and etching processes, which largely reduces the complexity and contamination during the fabrication process. In this section, the selective area growth of self-assembled quantum dots on Si developed by Choi et al. will be introduced [23].

The preparation step before the growth was similar to that of the other SAE process. A 20 nm thick SiO<sub>2</sub> layer was deposited on the (100) Si substrate with an e-beam assisted sputter. Then, a 10-nm-thick polymer e-beam photoresist was coated on the SiO<sub>2</sub> layer. E-beam lithography was used to define the growth area with the acceleration voltage of 35 keV, the line dose of 1.2-1.35 nC/cm and the probe current of 5 pA. The developing time of the methylmethacrylate photoresist was 90 seconds. The oxide was etched by reactive ion etching with CF<sub>4</sub>. The gas flow rate and pressure were 25 sccm and 50 mTorr. After the patterning of the oxide mask, the wafer was loaded into the MOCVD growth chamber. The wafer was heated

up to 800 °C for 10 min for annealing the damage caused by the reactive ion etching and removing the residual oxide.

The Stranski-Krastanov growth was initiated with a 2D layer growth of InAs. After reaching the critical thickness, the self-assembled quantum dots started to form. After the 6 seconds growth of the quantum dot layer at 430 °C, the growth was interrupted by 30 seconds to let the



**Figure 3.6** SEM image of the selective area grown InAs quantum dots on silicon substrate quantum dots experience an Ostwald ripening process, in which smaller InAs islands formed larger InAs islands [64],[65].

The SEM image of the selectively grown InAs quantum dots on Si substrate is shown in Figure 3.6 [23]. From the SEM image, quantum dots with an average diameter 30 nm could be observed. The density of these quantum dots was  $1 \times 10^{11} \text{ cm}^{-2}$ . The SEM image also showed that no quantum dot was formed on the SiO<sub>2</sub> mask area.

The research performed by Choi et al. demonstrated the selective growth of InAs quantum dots on Si substrates with SiO<sub>2</sub> masks. They found SiO<sub>2</sub> was an efficient mask material

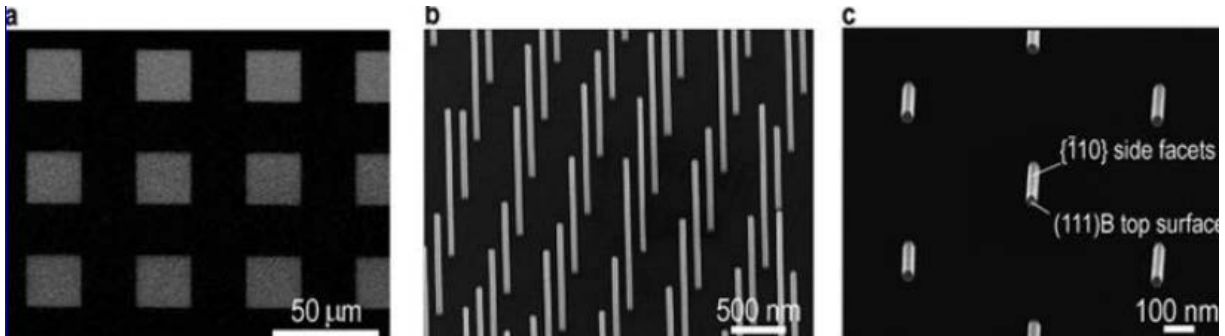
for selective quantum dot growth. However, the uniformity of their quantum dots needs to be improved and the regrowth techniques also need to be further developed in order to fabricate device quality quantum dots with this selective area growth technology.

### 3.3 Nanowires

The growth of III-V material nanowires on Si substrates had been studied by researchers for many years. Besides the typical advantages provided by integrating III-V materials on Si substrate, the one dimensional vertical nano-architecture and fast electron mobility of such nanowires allow for fabricating low power consumption and ultrafast electronic devices with high integration density on Si circuits [66],[67],[68],[69],[70],[71],[72]. In addition, the III-V nanowires can be grown directly on Si substrate without any surface passivation or buffer layers even though the lattice mismatch between the III-V material and the Si substrate can be quite large [73]. However, the uncontrollable growth direction caused by the polar on non-polar nature of the two materials was a big issue for III-V vertical nanowire growth on Si. The III-V nanowires have a zinc-blende structure which enables their growth on  $\langle 111 \rangle$  A or  $\langle 111 \rangle$  B directions. For Si,  $\langle 111 \rangle$  A and  $\langle 111 \rangle$  B directions are equivalent, because Si crystal is non-polar. However, for zinc-blende III-V materials, their polar crystal structure resulted in four growth directions along  $\langle 111 \rangle$  happening simultaneously on the Si substrate when the growth started. Only one of the four directions was perpendicular to the surface of the Si substrate. The inclined growth of nanowires resulted in lower nanowire density. Therefore, controlling the nanowires to grow perpendicular to the substrate was a crucial problem to be solved [66]. In this section, an example of how to control the growth direction of the vertical III-V nanowires on Si substrate will be introduced. This research utilized selective area epitaxy, which reduced

the threading dislocations caused by thermal expansion coefficient difference in the epitaxial interface [74].

In the report of Tomioka et al., the InAs vertical nanowires were successfully grown directly on the Si surface [75]. They first used amorphous material, i.e. SiO<sub>2</sub>, as the mask for growth, and patterned the mask with e-beam lithography. The patterned features were 20  $\mu\text{m}$   $\times$  20  $\mu\text{m}$  squares of hexagonal cross-section openings with the diameter about 60 nm and pitch about 400 to 800 nm. The InAs nanowires were grown by LP-MOCVD at about 76 Torr. A thermal cleaning was performed in a H<sub>2</sub> ambient at 925  $^{\circ}\text{C}$ , and the growth was performed at 540  $^{\circ}\text{C}$  for 20 min. Figure 3.7 [75] shows the result of the experiment.



**Figure 3.7** Image of (a) the square pattern of nanowires, (b) the low magnification view of the InAs nanowires, and (c) the close view of the InAs nanowires

The InAs nanowires were grown at the openings of the mask defined by the e-beam lithography, which are about 3  $\mu\text{m}$  tall, 60 nm in diameter and 400 to 800 nm pitch.

In order to obtain this vertical growth result, the wafer was carefully engineered before the growth started. According to the material property, researchers found that the nanowire grown on the (111) A plane on the Si surface would lead to inclined growth while those grown on the (111) B plane would result in vertical growth. They also found that if the (111) A plane was treated by As and In atoms and formed the In-terminated Si<sup>1+</sup> or As-incorporated Si<sup>3+</sup>, the

(111) A plane would become equivalent to the (111) B plane. Therefore, after the 5 min 925 °C thermal cleaning in H<sub>2</sub> environment, the wafer was cooled down to 400 °C, and AsH<sub>3</sub> was flowed into the chamber to form As-incorporated Si<sup>3+</sup>. Then, a flow-rate modulated epitaxy mode was employed in the MOCVD [76]. The flow-rate modulated epitaxy alternated the group III and V precursor supply in the MOCVD. This was to enhance the termination of In and As atoms to the Si surface, which formed more of the (111) B equivalent surface planes and resulted in the vertical growth of InAs nanowires. The result of this growth technique was impressive. It increased the percentage of vertical InAs nanowires grown on Si substrate from approximately 31% to about 95%.

The research introduced above solved the direction control problem of vertical III-V nanowire growth on Si substrates. It utilized selective area epitaxy technology to increase the quality of the epitaxial nanowires. It set the foundation for growing nanowires formed by more desirable III-V materials such as GaAs and GaN on Si substrates.

In this chapter, monolithically fabricated LED, quantum dots and nanowires were introduced to illustrate how to apply the SAE techniques we discussed in previous chapters to integrate novel III-V devices and structures on Si substrate. From these examples, we can see the monolithic integration of III-V devices on Si is a promising but complicated technology. A lot of issues still need to be solved in the fabrication process in order to successfully fabricate III-V devices without damaging or contaminating the other parts of the substrates and to integrate the III-V and Si parts of devices to make them work properly together and fully functional. In the fabrication process of monolithic III-V on Si devices, the role of selective area epitaxy is to simplify the complicated process and to increase the quality of the epitaxial layers. These



advantages made selective area epitaxy technology the choice of many research groups in this field.

## 4. CONCLUSION

This thesis provides a detailed review of the III-V semiconductor on Si substrate SAE growth technology. The motivations to develop this technology and the historical review are introduced in Chapter 1. In Chapter 2, the typical growth methods of III-V SAE on Si using both MOCVD and MBE are provided. In addition, the solutions to some of the issues surrounding in these growth techniques are discussed. Monolithically fabricated III-V on Si devices and nanostructures by SAE are introduced in Chapter 3.

The information provided in this paper shows that the III-V on Si SAE technology is a promising growth technology to integrate III-V materials on Si to realize original and innovative device structures and concepts. It decreases the complicity of fabricating high dimensional structures such as quantum dots and nanowires, and at the same time increases the quality of the epitaxial layers. The theoretical study of the issues of this technology in the late 1980s laid the foundation for its improvement during the past 20 years. Nowadays, some high quality devices are already fabricated by III-V on Si SAE. It is also a technology that has big potential. The development and application of III-V on Si SAE in quantum dot and nanowire growth makes it a popular candidate for high speed electronic and monolithic optoelectronic device fabrication in the future.

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